Product Specification

AU OPTRONICS CORPORATION

(   ) **Preliminary Specification**
(V) **Final Specification**

Module	14.0" (13.97") HD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B140XW02 V1 (3A)
Note (🔘)	*LED Backlight with driving circuit design*

Customer	Date	Approved by	Date
Sony		Bonnie Chen 07/10/2009	
Checked & Approved by	**Date**	**Prepared by**	**Date**
		Jonken Fan 07/10/2009	

Note: This Specification is subject to change without notice.

NBBU Marketing Division
AU Optronics corporation

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1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.

6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.

7) Do not open nor modify the Module Assembly.

8) Do not press the reflector sheet at the back of the module to any directions.

9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.

11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.

13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electronic breakdown.

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2. General Description

B140XW02 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B140XW02 V1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

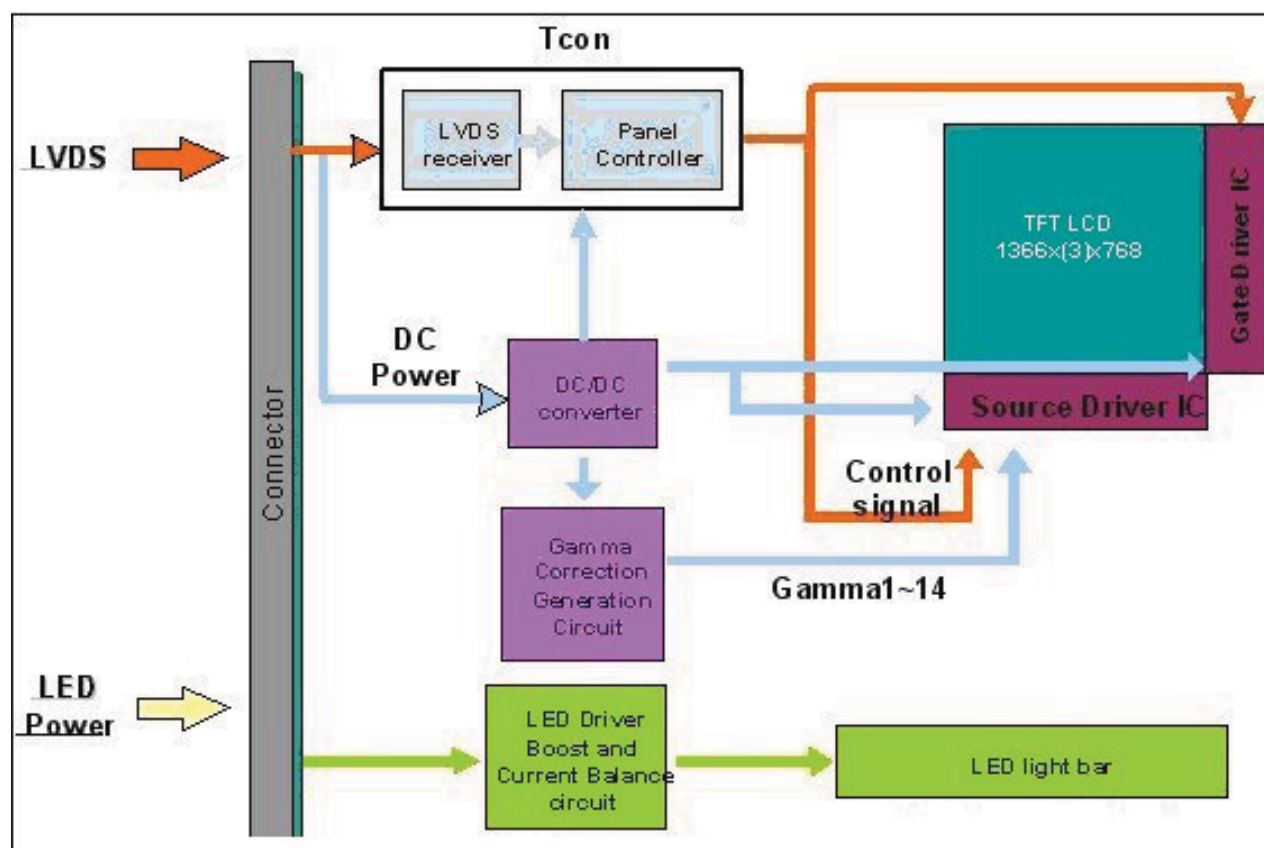| Items	Unit	Specifications			
Screen Diagonal	[mm]	354, 14.0"(13.97")			
Active Area	[mm]	309.399 x 173.952			
Pixels H x V		1366 x 3(RGB) x 768			
Pixel Pitch	[mm]	0.2265 x 0.2265			
Pixel Format		B.G.R. Vertical Stripe			
Display Mode		Normally White			
White Luminance (I_{LED}=20mA) **(Note: ILED is LED current)**	[cd/m^2]	200 typ. (5 points average) 170 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		500 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.5 max. (Include Logic and Blu power)			
Weight	[Grams]	320 max.			
Physical Size **Include bracket**	[mm]		Min.	Typ.	Max.
		Length	319.9	320.4	320.9
		Width	204.6	205.1	205.6
		Thickness	-	-	3.6
Electrical Interface		1 channel LVDS			
Glass Thickness	[mm]	0.5			
Surface Treatment		Glare, Hardness 3H, Reflection 4.3%			

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3. Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches wide Color TFT/LCD 40 Pin one channel Module

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4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[^{o}C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[^{o}C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).
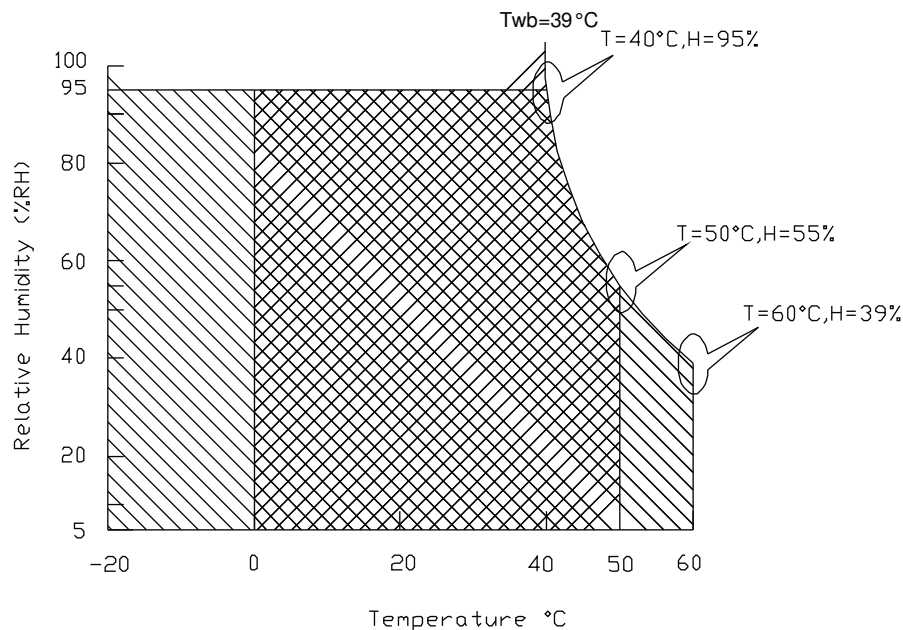
Operating Range   Storage Range

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5. Electrical Characteristics

5.1 TFT LCD Module

#### 5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1	[Watt]	Note 1
IDD	IDD Current	-	-	333	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2：Measure Condition
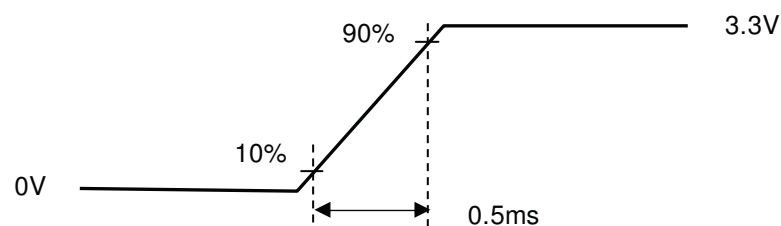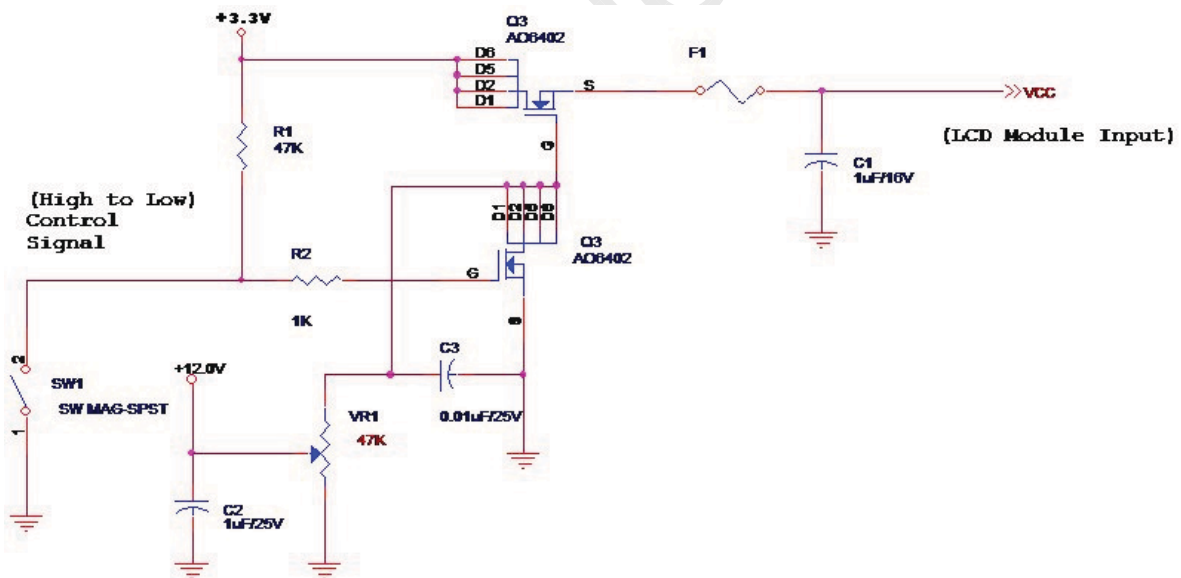
Vin rising time

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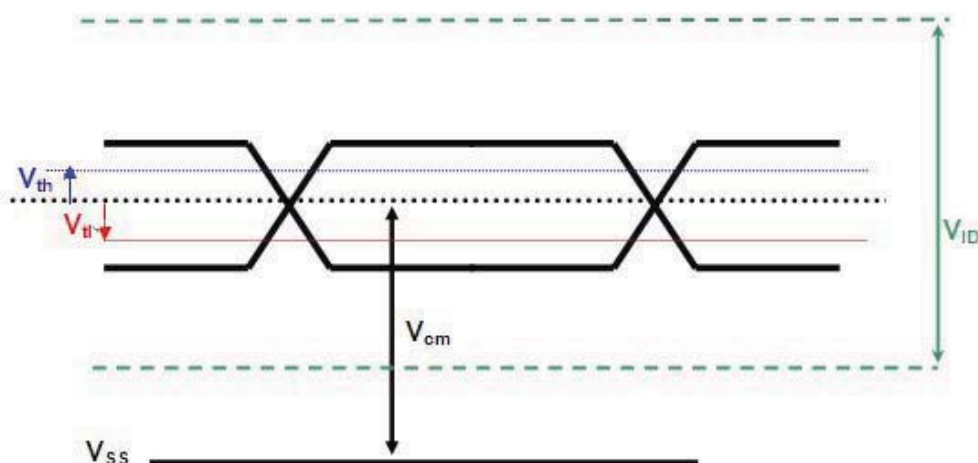
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5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{th}	Differential Input High Threshold (Vcm=+1.2V)	-	100	[mV]
V_{tl}	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
V_{ID}	Differential Input Voltage	100	600	[mV]
V_{cm}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform

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5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	3.5	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	12,000	-	-	Hour	(Ta=25℃), Note 2 I_F=20 mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

**Note 2:** The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	7.0	12.0	21.0	[Volt]	
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	100	-	20K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

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6. Signal Interface Characteristic

6.1 Pixel Format Image

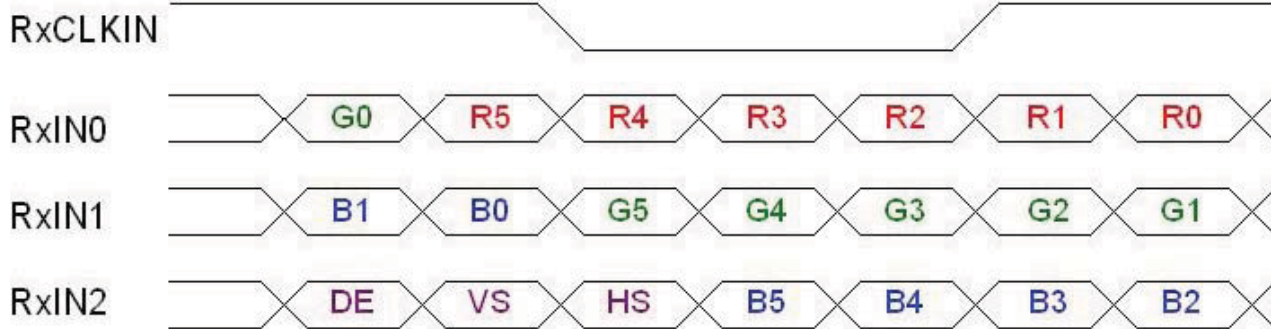Following figure shows the relationship of the input signals and LCD pixel format.
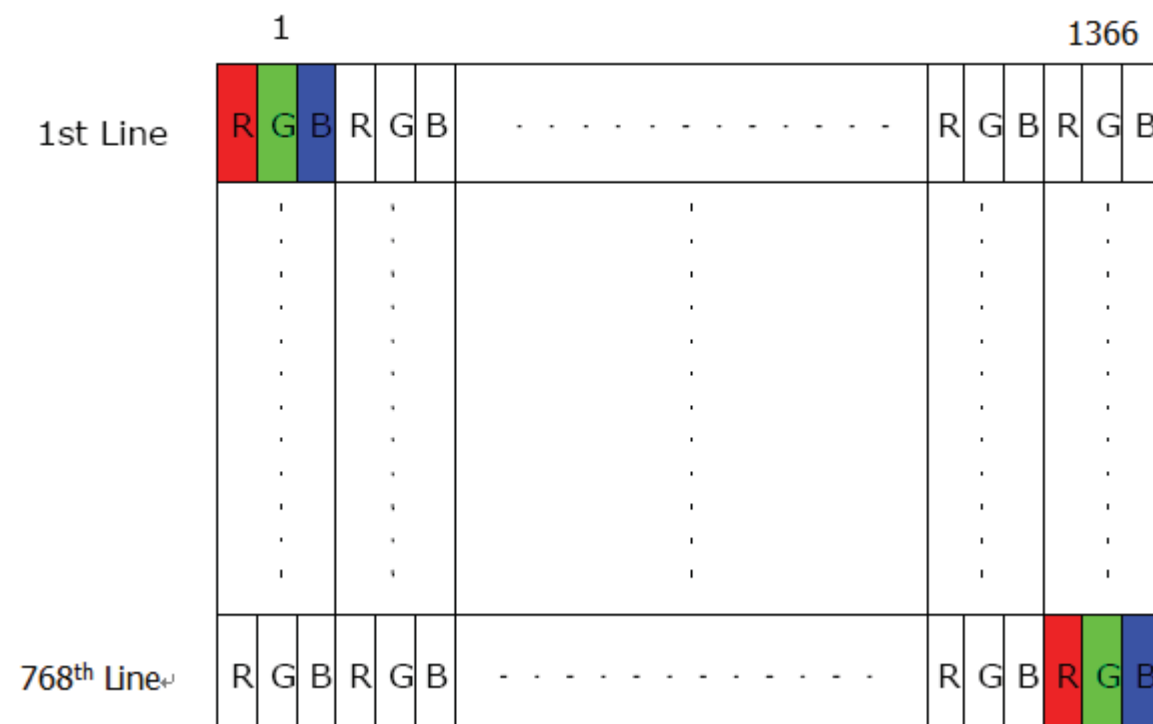
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6.2 The Input Data Format

Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

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6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20455-040E-12A or compatible
Mating Housing/Part Number	IPEX 20453-040T-11 or compatible

6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

B140XW02 V1		
Pin	Signal	Description
1	NC	No Connection (Reserve)
2	VDD	PowerSupply,3.3V(typical)
3	VDD	PowerSupply,3.3V(typical)
4	DVDD	DDC 3.3Vpower
5	NC	No Connection (Reserve)
6	SCL	DDC Clock
7	SDA	DDC Data
8	Rin0-	-LVDS differential data input(R0-R5,G0)
9	Rin0+	+LVDS differential data input(R0-R5,G0)
10	GND	Ground
11	Rin1-	-LVDS differential data input(G1-G5,B0-B1)
12	Rin1+	+LVDS differential data input(G1-G5,B0-B1)
13	GND	Ground
14	Rin2-	-LVDS differential data input(B2-B5,HS,VS,DE)
15	Rin2+	+LVDS differential data input(B2-B5,HS,VS,DE)
16	GND	Ground
17	ClkIN-	-LVDS differential clock input
18	ClkIN+	+LVDS differential clock input
19	GND	Ground
20	NC	No Connection (Reserve)
21	NC	No Connection (Reserve)
22	GND	Ground
23	NC	No Connection (Reserve)

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24	NC	No Connection (Reserve)
25	GND	Ground–Shield
26	NC	No Connection (Reserve)
27	NC	No Connection (Reserve)
28	GND	Ground–Shield
29	NC	No Connection (Reserve)
30	NC	No Connection (Reserve)
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No Connection (Reserve)
35	PWM	System PWM Signal Input
36	LED_EN	LED enable pin(+3V Input)
37	NC	NC for DCR Enable only
38	VLED	LED Power Supply 7V-21V
39	VLED	LED Power Supply 7V-21V
40	VLED	LED Power Supply 7V-21V

<BACK VIEW>
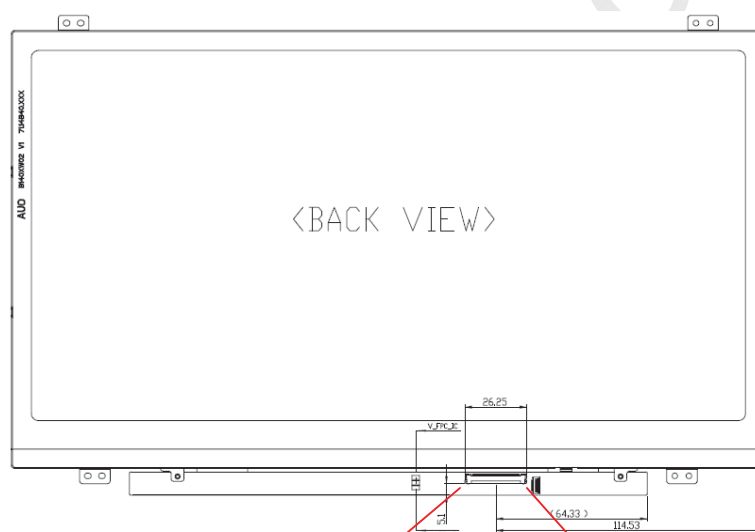
Signal Pin40   **Signal Pin1**
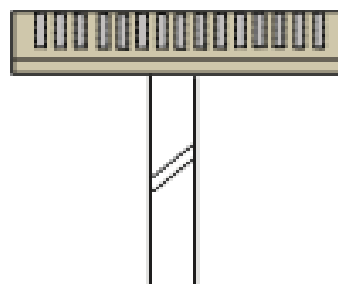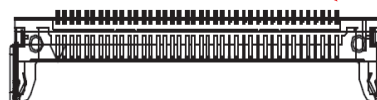
Note1: Input signals shall be low or High-impedance state when VDD is off.

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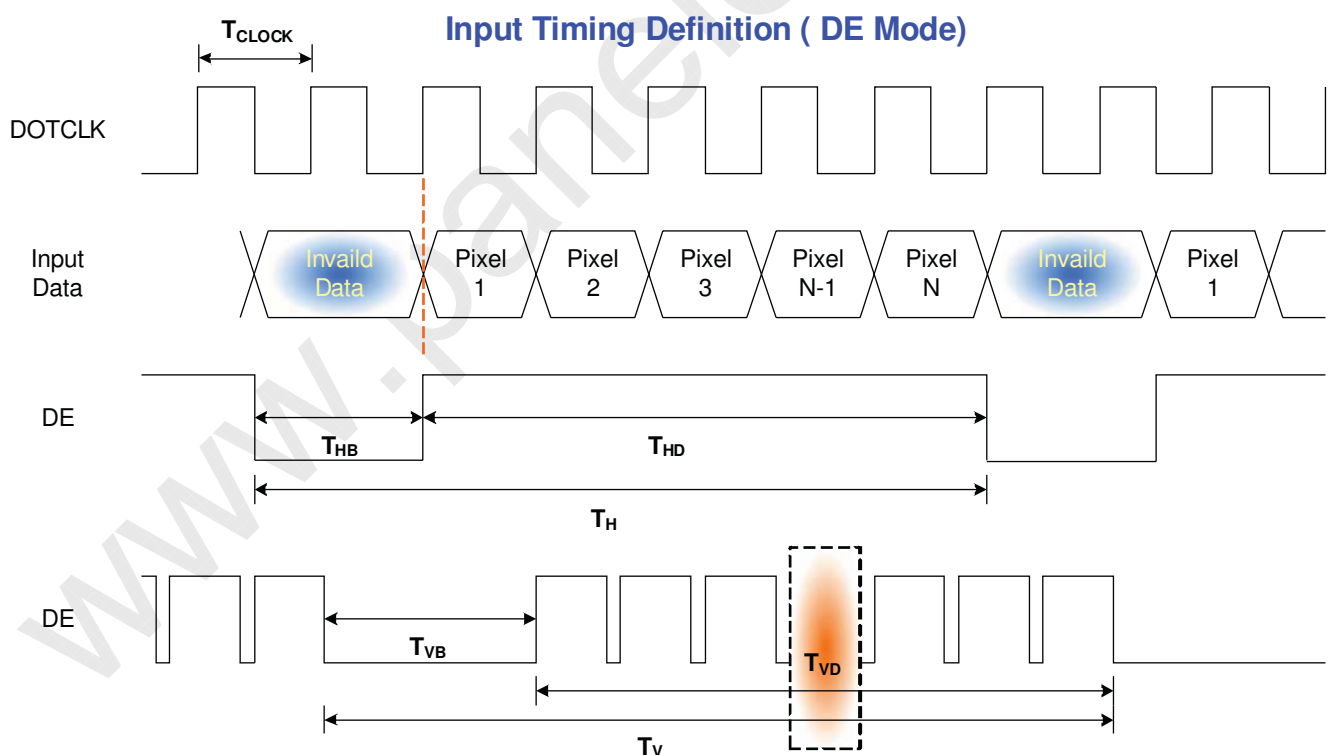
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6.4 Interface Timing

6.4.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T_{Clock}	-	72	-	MHz
Vertical Section	Period	T_V	780	803	1023	T_{Line}
	Active	T_{VD}		768		
	Blanking	T_{VB}	12	35	255	
Horizontal Section	Period	T_H	1406	1494	2047	T_{Clock}
	Active	T_{HD}		1366		
	Blanking	T_{HB}	40	128	681	

Note : DE mode only

6.4.2 Timing diagram

Input Timing Definition (DE Mode)

T_{CLOCK}

DOTCLK

Input Data

| | Invaild Data | Pixel 1 | Pixel 2 | Pixel 3 | Pixel N-1 | Pixel N | Invaild Data | Pixel 1 | |

DE

T_{HB}　　T_{HD}

T_H

DE

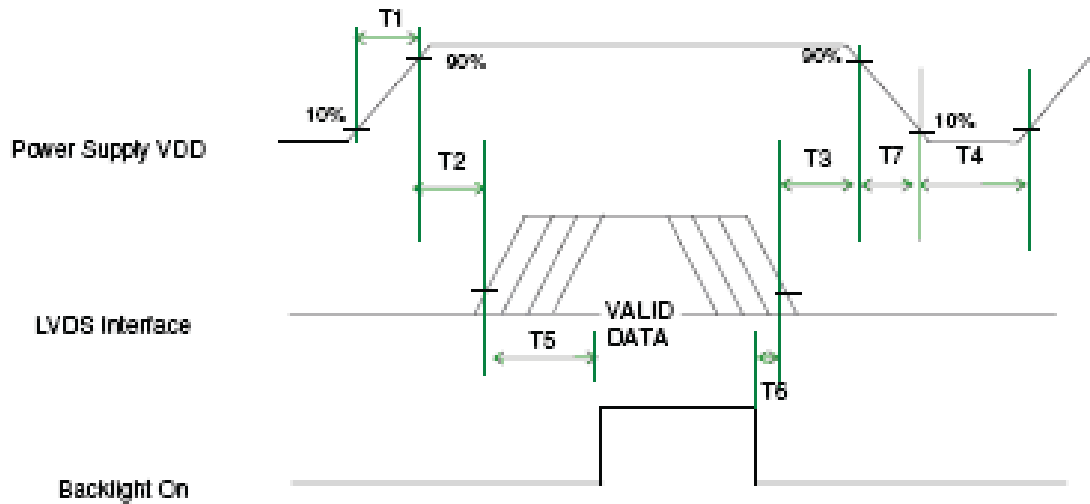T_{VB}

T_{VD}

T_V

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6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

Power Sequence Timing

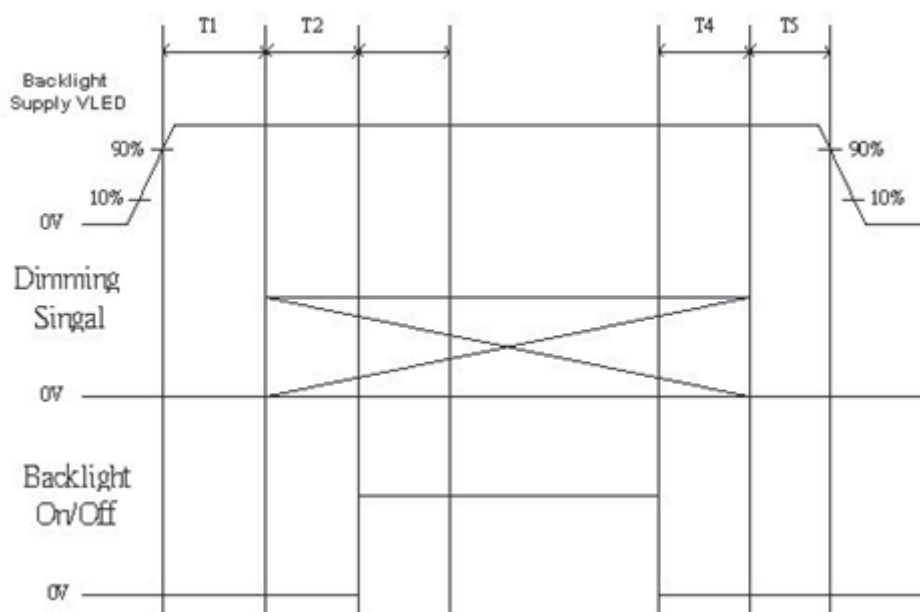| Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	
T2	0	-	50	
T3	0	-	50	
T4	400	-	-	ms
T5	200	-	-	
T6	200	-	-	
T7	0	-	10	

Note:If T3,T5,T6 couldn't match above specifications, must request T3+T5+T6 > 200ms at least
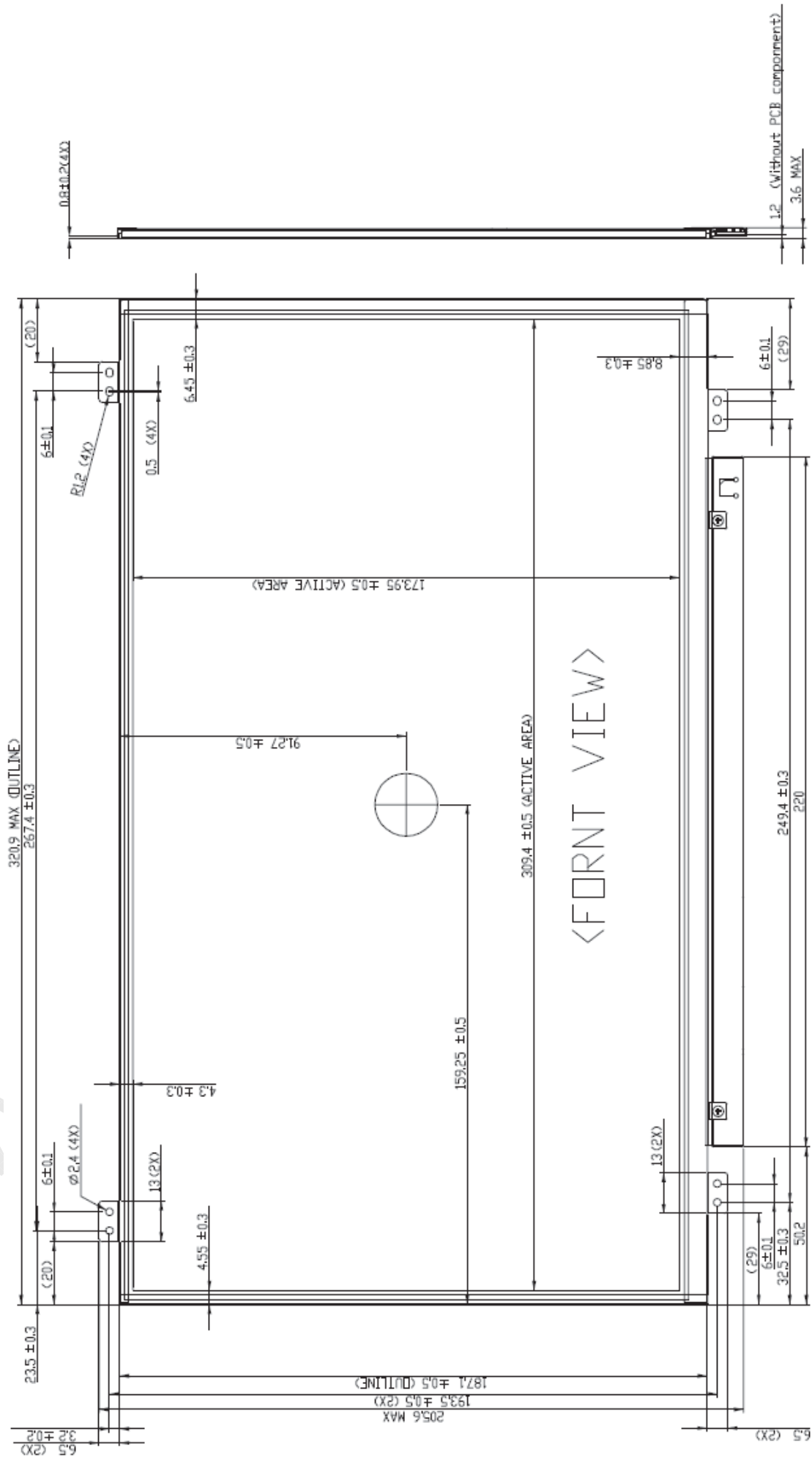
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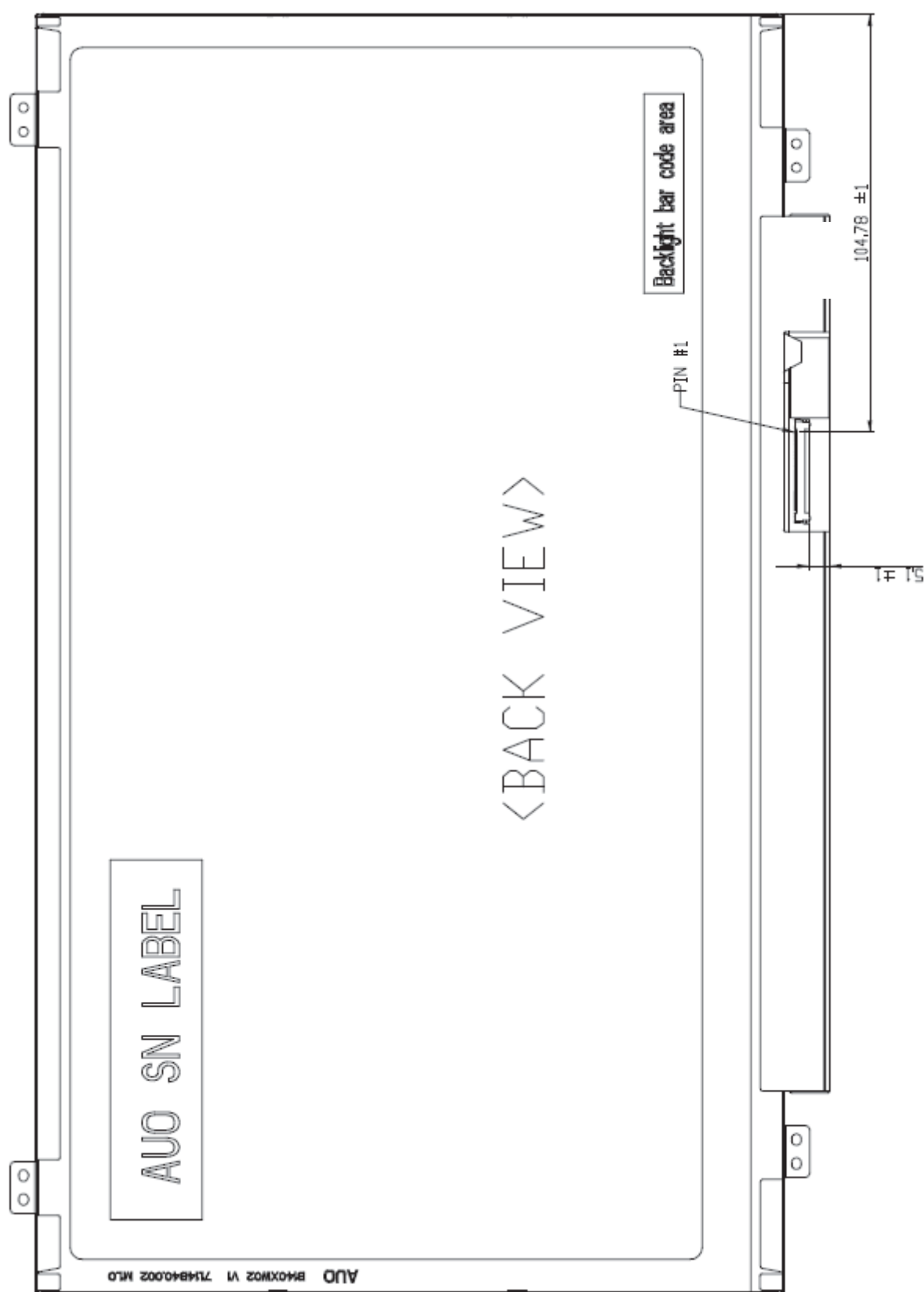LED on/off sequence is as follows. Interface signals are also shown in the chart.

Symbol	Values			Unit
	Min	Typ	Max	
T1	10	---	---	ms
T2	10	---	---	
T4	0	---	---	
T5	10	---	---	

8. Mechanical Characteristics
8.1 LCM Outline Dimension

<BACK VIEW>

Backlight bar code area

PIN #1

104.78 ±1

5.1 ±1

AUO SN LABEL

AUO   B140XW02 V1 71.14B40.002 MLD

Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

B140XW02 V1   Document Version : 1.0

9. Shipping and Package

9.1 Shipping Label Format

Week code

Model name

Manufactured XX/XX
Model No: **B140XW02** V.1
Limited Warranty
MADE IN CHINA (S1)

H/W: 3A F/W: 1

c UL us (Pb)
E204356

RoHS

15

H/W
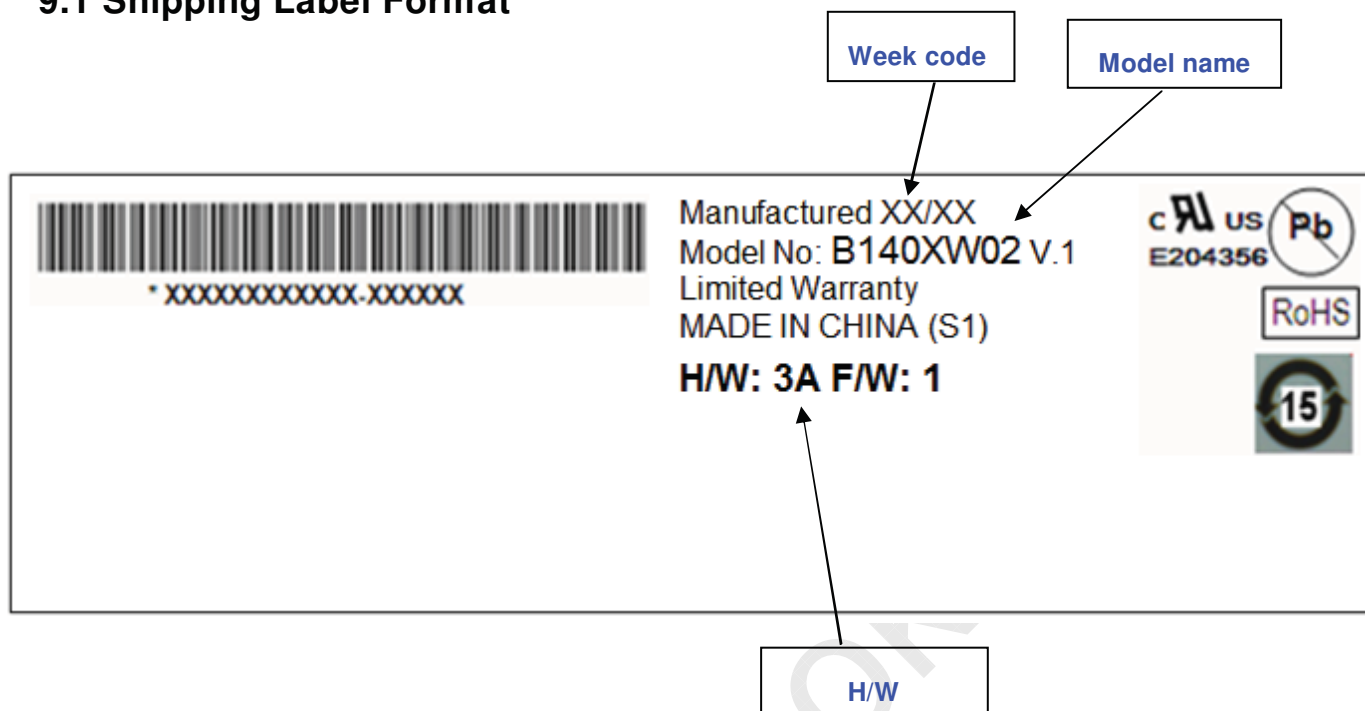
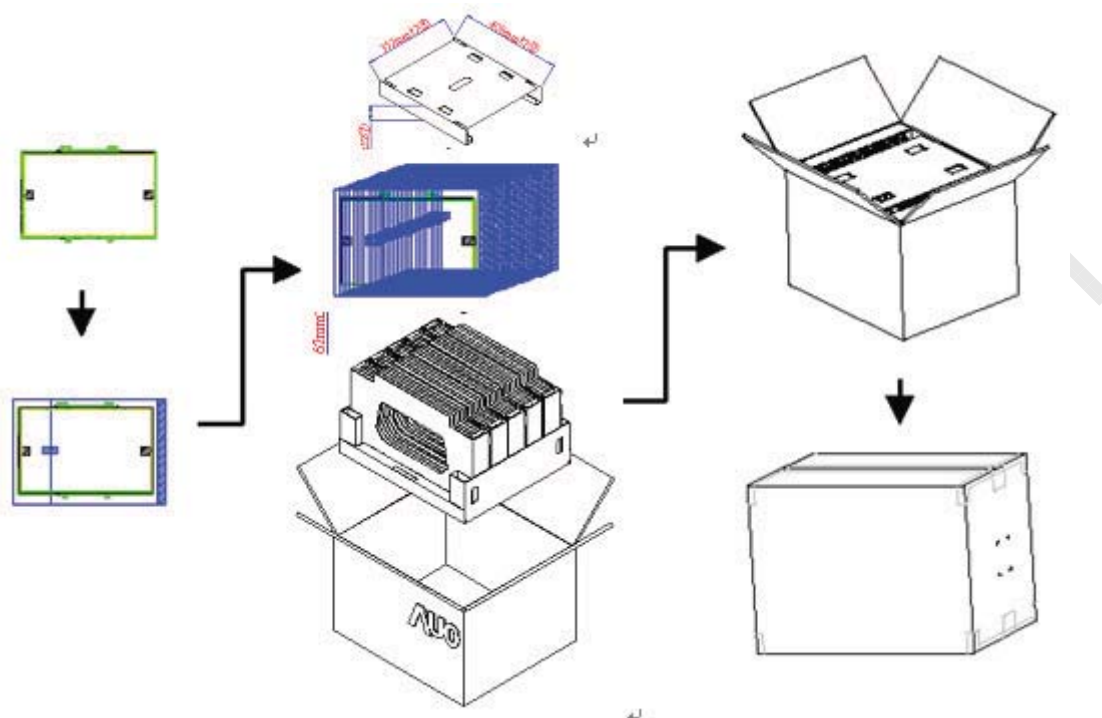## 9.2 Carton Package

The outside dimension of carton is 455 (L)mm x 380 (W)mm x 355 (H)mm

9.3 Shipping Package of Palletizing Sequence